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Analysis and Design New Double-Tail Comparator for Offset Voltage Optimization

Kavindra Pal[1*], Dr. Anuj Garg[2]
The Lakshmi Narain College of Technology Madhya Pradesh 462022[1]

The Lakshmi Narain College of Technology Madhya Pradesh 462022[2]

Abstract

This High-performance Comparator circuits are required and important modules for the design of integrated circuit data converter architectures that will be used in a variety of wireless portable electronic systems, including Smart phones and tablets. Using two alternative designs, the Double-Tail Comparator work reported in this study investigates specifications such as offset voltage (mv), power dissipation (W), voltage gain (dB), kick back noise reduction, propagation latency (ps), and speed-power product, among others (fJ). Analysis and Design New Double-Tail Comparator for Offset voltage optimization. A complete study and simulation of two comparator circuits is presented in this paper. The work is performed using the 0.13-micron CMOS process technology. For the comparator circuit, an integrated circuit designer can completely balance trade offs such as power consumption reduction, circuit speed optimization, and offset voltage minimization by using a hybrid design approach.

Keywords

Double-Tail Comparator, Data converter architectures.

Introduction

Comparator is one of the fundamental building blocks in most of the analog-to-digital converters (ADCs). Many of the high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub-micrometer (UDSM) CMOS technologies suffer from very low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [2]. Hence, designing of high-speed comparators is more challenging when supply voltage is smaller. In other words, in this technology, to achieve high speed, larger transistors are required to compensate the reduction of the supply voltage, which also means the more die area and power is needed. Besides, low-voltage operation results in the limited common mode input range, which is important in high-speed ADC architectures, such as flash ADCs. The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison. Vp is the input voltage (pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. High speed dynamic regenerative comparators are used in low power and area efficient analog to digital converters to improve speed and power efficiency. Speed and power consumption are the two factors that define the comparators accuracy. A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. In this research work, a new double tail comparator is proposed by modifying the low voltage low power double tail comparator circuit for power efficient and high speed operation. In the proposed dynamic double tail comparator System both the power dissipation and delay time would be significantly reduced. The simulations are carried out in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology

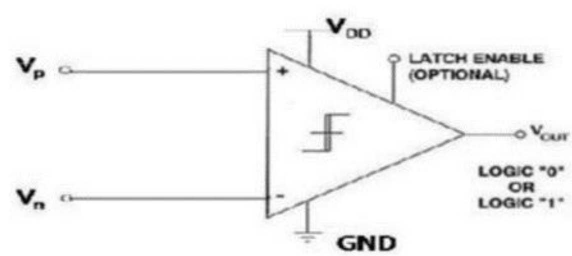

Figure 1: Schematic of Comparator

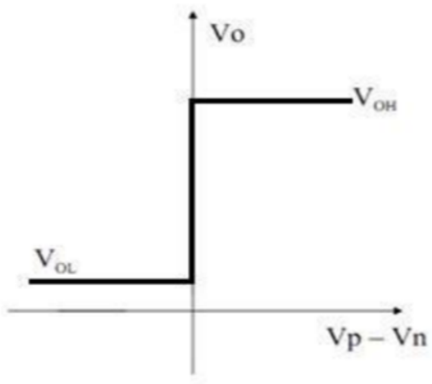

Figure 2: Ideal voltage transfer characteristic of comparator

A timed comparator is composed of two stages in most instances. The first stage consists of connecting the two input signals together. Two cross-coupled inverters are used in the second stage (regenerative stage), with each inverter's input connected to its output on the other inverters. C MOS-based latches consume very little static power during the regeneration step and its subsequent phases [3, which is due to the power ground route being switched by either an NMOS or PMOS transistor]. In many applications, the speed of the comparator, the amount of power dissipated, and the number of transistors are more essential. For example, if the speed of the comparator is important, the regeneration stage could be built to start its function halfway between the power supply and the ground. For example, in a typical comparator, the static power consumption decreases; as a result, the transistor count increases, resulting in a reduction in the comparator's speed.

Related work

K. Dubey et al.[1] The offset control method and comparator core have been modified to reduce leakage through the bulk node and other design flaws. High-speed, low-power phase detectors and charge pumps are also proposed.

S. R. Vemu et al.[2] When the threshold voltages (Vt) of the devices are not scaled at the same speed as the rail voltages of the latest CMOS technology, fast comparators in CMOS have the problem of having less rail voltages. When compared to other forms of comparators, the suggested approach uses around 290mW less power.

The leakage current, static power, and dynamic power are greatly reduced by S. S. Chiwande et al[3] the proposed structure of Double Tail Comparator.

The circuits are modeled with 180nm CMOS technology in cadence virtuoso by S. S. Baghel et al[4]. DRC and LVS checks are used to do post-layout analysis on the circuit.

G. Puvaneswari et al.[5] use control transistors and NMOS switches to modify the traditional double tail regenerative comparator. The improved comparators' power and delay are investigated for use in high-speed ADCs.

A. Khorami, et al.[6] present a comparator in which the Pre-Amplifier is turned off when the maximum gain is reached, ensuring that the latch receives the greatest potential gain at all times.

S. Srivastava and colleagues[7] An approach of double tail comparator with a technique of regenerative inverter is introduced in this work, which is an important basic component of ADCs, and the result is proven by post layout simulation on 180 nm CMOS Technology.

Proposed methodology

In the development of advanced CMOS technologies, compact mathematical models are needed that can model the device physics accurately. The removal of the complexities and improve the feasibility of available mathematical models particularly in view of quantum mechanical effects for the development of advanced MOSFET devices.

Extend the development of an analytical, potential-based and predictive compact model for threshold voltage for nano scale JL-DG CMOS, which can further to junction based devices. The models derived may be suitable for circuit simulators.

The silicon dioxide (SiO_2) is main material used for gate oxide layer. The scaling of the SiO_2 gate oxide layer and finding a better alternative is required. Because it suffers from problems such as large leakage currents due to direct tunneling of electrons from gate to channel, large power dissipation and difficult fabrication process.

The characterization of JL-DG CMOS for an improved parametric performance like drain current, I_{ON}/I_{OFF} ratio, DIBL, sub threshold swing, and trans conductance using metal gates and high- κ spacers.

Offset

The offset voltage is solitary the prime design metrics of a dynamic latch employed in the voltage comparator. The offset voltage is the crucial requirement for accuracy of the comparator; method for its estimation is of immense significance to the designer. The offset can be divided into static and dynamic component. For the comparator, decision threshold is ideally.

The decision threshold shifts away from zero due to component mismatch and other non-ideal conditions. The offset voltage is defined as the amount for which the decision threshold shift

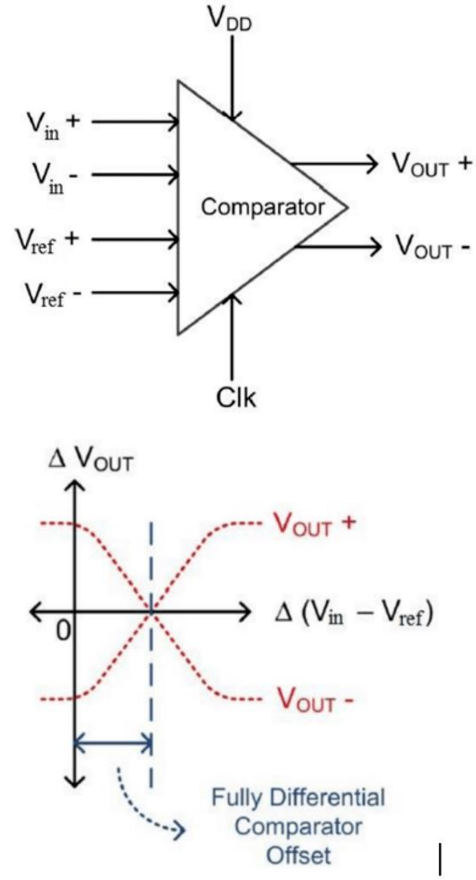

Figure 3 : Effect of Offset in Fully Differential Comparator

The effect of offset in fully differential comparator. The offset voltage restricts the comparison accuracy due to process variation in latched comparators. The offset voltage of the comparator can be reduce by coupling Pre-Amplifier stage before output latch, thus a precise Pre-Amplifier topology is essential, making it feasible to employ the comparator for high resolution purpose.

Power

In high performance battery powered systems, power is one of the most serious limitations. Nowadays, power efficient design is the main trend in the design of electronic circuits. There has been mounting need for the advancement of low voltage and power efficient circuits. To enhance the battery life, power efficient design is of great interest. The requirement of compact size and light weight demand the use of few batteries as possible owing to low voltage operation.The three different sources demand for low voltage systems: to extend battery life and a less amount of battery cells to decrease the volume and weight of the system due to rapid advent of battery operated portable systems needs optimum power for maximum performance. As a larger number of transistors are integrated on a single die reduction in power dissipation is further driven. A comparator is one of the essential components of many of the devices which are portable and hand held high speed devices that requires power efficiency.

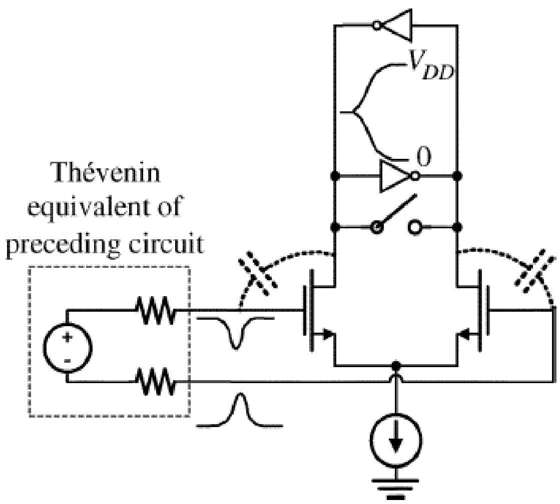

Figure 4: high speed devices that requires power efficiency

Designing high performance comparator is more challenging at lower supply voltage. The low power implementation is benefited from technology scaling; low supply voltage leads to less transistor currents and thus larger delay. To achieve high speed, transistor with bigger size is necessary to compensate the reduction of supply voltage which leads to more area and more power. Static comparators suffer from low speed and high power. To optimize power and speed dynamic comparators were proposed. The input voltage is disturbed because the circuit prior to it does not have zero output impedance which may deteriorate precision of the converter and the fastest and most power efficient comparators produces more kickback noise . Although, source followers are effective but adds static consumption dropping the power efficiency .

Moreover the voltages at the drains change significantly; generating kickback noise due to restrain current flow in the differential pair transistors, which go into the Triode region. The concept of Pre-Amplifier with MOS switches introduced at the inputs of the comparator and opened during the regeneration phase is still in use thereby reducing the kickback noise during that phase by sampling and isolating the input nodes during that phase (Singh, S., 2015) (Kim, S., et al., 2001). However, the value being applied differs from the previously sampled voltage when.

Power-Delay Product

High-speed performance and maximum power efficiency are well-known to be mutually exclusive trade-offs, and this is also true for the comparator. Speed optimization (low IJp) can be achieved at the expense of greater power consumption. developed a method for achieving a conciliation between these two opposing trade-offs by utilizing the delay-power product. In the majority of circuits, there is a trade-off between speed and power. As a result, the PDP is considered to be the superior design metric for performance comparison. The value of PDP must be kept as low as possible in order for the circuit to be effective.

Conclusion and future work

A detailed delay and power analysis for clocked dynamic comparators is performed, and two common topologies of conventional dynamic comparator and conventional double-tail dynamic comparators are studied and assessed. In addition, a new dynamic comparator with low-voltage low-power capability was presented based on theoretical calculations in order to increase the comparator's performance. Detailed analysis of performance parameters for traditional dynamic latch comparators (referred comparators), including the single tail current dynamic latch comparator (STDLC), double tail current dynamic latch comparator (DTDLC), modified double tail current dynamic latch comparator (MDTDLC), two-stage dynamic comparator without an inverted clock (DTDLC-CLK), and Pre-Amplifier with latch comparator Various reset strategies for dynamic latch comparator are also reviewed and studied, and a novel reset technique (shared charge logic) is presented based on this research to increase the comparator's speed and power. To increase the performance parameter of the dynamic latch comparator, a novel comparator architecture with shared charge logic is developed. The performance parameters are also given analytical expressions. All of the referred comparators, as well as the suggested comparator, were simulated in Cadence Virtuoso Analog Design Environment using 90 nm CMOS technology and a supply voltage of 1 V.

Because speed, power consumption, PDP, and die area are all performance trade-offs, they are mostly simulated for the suggested.In this research, the comparator circuits were investigated. With greater dynamic range, the designs are primarily tuned for propagation delay, offset, and power. Many obstacles in comparator design must be overcome in order to produce a system with high performance and desirable attributes. A high-resolution, high-speed, power-efficient comparator is the bottleneck in high-performance applications like ADCs. The proposed circuit construction has a promising and optimum performance for offset, power, and speed. The circuit structure's key highlights are power efficiency and conversion speed with low offset voltage. The circuit configuration of will allow designers to explore and expand design space with new possibilities in order to increase speed and efficiency. The fully differential double tail dynamic comparator has a low propagation delay, low offset voltage, and no offset calibration approaches, which necessitates additional devices, calibration time, and power-hungry design strategies.

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- Full name-Dr. Anuj Garg
- Email-anuj.garg@lnct.ac.in
- Phd. With Sub/topic -Solar Energy Harvesting Method by MPPT for Telecom Industry
- Specialization-Electronics & Communication
- No. of research paper published national /international

1. Communications on Applied Electronics 5(7):1-4, July 2016
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- Achievements -Chapter Chair CII –Yi Bhopal (2020-21)10.
- Total work experience19+years

- Full Name-Kavindra Pal
- Email-kavindrapalak1993@gmail.com
- M.tech with Branch-VLSI Design(2021)
- Key Skills -Detailed oriented, hardworking electronics engineer who performs the best in challenging environment, with solid knowledge in Front-end VLSI design flow with very good experience in HDL modelling using Verilog, In addition to good knowledge in digital electronics, Computer organization, CMOS circuits, STA and ASIC design Flow.