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Design of Low Power 4:2 Compressor for Multipliers

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Abstract

In this paper, energy-efficient design for a 4:2 compressor is examined which utilizes 28 transistors. This design further enhances the XOR-MUX architecture for the 4:2 compressor and lowers the power consumption of the compressor. The methodology used for designing this architecture is CMOS modelling, in which each module of the architecture is designed using the least number of CMOS transistors. The proposed design of the compressor, when implemented on 45nm technology using the Microwind tool, provided a maximum output delay of 650ps and lowered the number of transistors utilized by 28% to 38%. This low power design will help the design of low energy and fast multipliers

Keywords

Multiplier, compressor, high speed, low power, XOR-MUX module

1.Introduction

In digital devices, the role of a multiplier is to multiply two n-bit numbers. It's an operation that's widely employed in electronic devices like digital measuring instruments, microprocessors, microcontrollers, etc. The current multipliers are of two types, serial multipliers which are small in size but are quite slow. On the opposite hand, we have parallel multipliers that take up a large area but provide high speed. Designing a multiplier that is of high speed and covers up less area is the requirement so modern-day devices may be both fast and small.

When it involves designing small multipliers the difference between the parameters of assorted designs is not much. The difference comes to light after we start moving towards high bit multipliers like 8 bit and more and designing new circuits for these multipliers are a highly lengthy and complex process and can result in large boolean equations. Thus the key to designing these multipliers is following the fundamental principles of VLSI i.e. regularity, modularity, and locality.

In parallel multipliers, there are various multipliers like Wallace tree multipliers which are very fast but take up a large area and are high in complexity. Then there are other designs like array multipliers which consume less area but have propagation delay more than Wallace tree multiplier.

To achieve the purpose where we have got less output delay and also the area covered by the module is also less the design of compressors comes up. Compressors are high-speed processing devices that are utilized in multipliers to cut back the quantity and size of modules used. The compressors utilized in multipliers are made by integrating two successive Full adders and minimizing their logic.

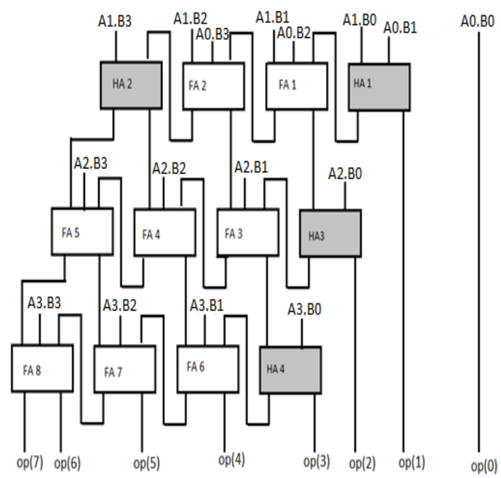

Fig 1: Design of an Array Multiplier

2.Compressors

A compressor is a combinational circuit that compresses the number of partial products to a lower number of partial products. For instance, a 4:2 Compressor compresses 4 partial products into 2 partial products [2]. A 4:2 Compressor is depicted by the diagram shown in Figure 2.

The role of a compressor in a multiplier is to decrease the quantity of circuitry within the module which results in lowering of the maximum output delay of the circuit. The compressor also results in a decrease in power consumption because the components utilized in the module is low. This compressor when replaces multiple modules of the multiplier results in a cascading effect within the decrease of the parameter values of the multipliers

A 4:2 compressor has 5 inputs M1, M2, M3, M4, and

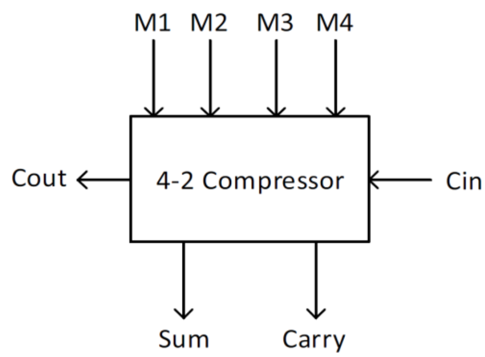

Fig 2: Block Diagram of Compressor

Cin where M1 to M4 are partial products and Cin is the carry obtained from a previous module. It consists of 3 outputs Cout, Carry, and Sum where Cout acts as carry for the upcoming module [3]. Figure 3 shows the architecture of the basic module of a compressor.

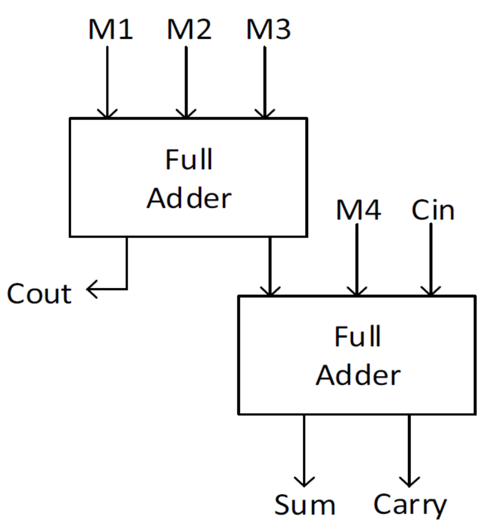

Fig 3: Basic Module of a 4:2 Compressor

In literature, various architectures have been referred to for implementation of a 4:2 compressor but the two that have been commonly used. The first one involves the use of XOR modules and a 2x1 MUX where there are three XOR modules and two 2x1 Multiplexer

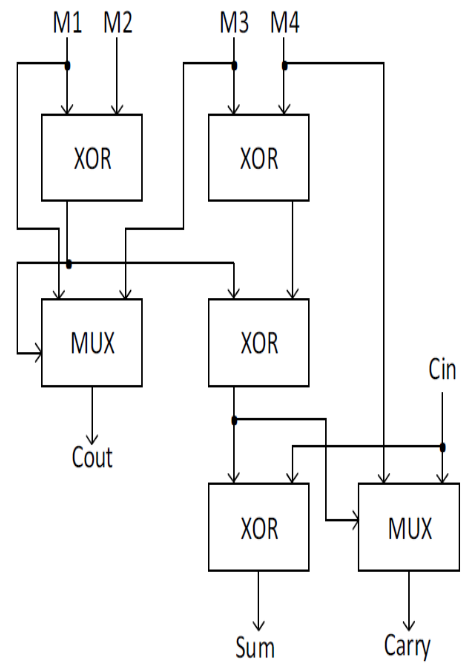

Fig 4: Architecture using XOR module

modules [4]-[7]. This architecture is denoted in Figure 4.

The other architecture of the 4:2 compressor involves the use of an XOR-XNOR module and 2x1 MUX where there are two XOR-XNOR modules and four 2x1 MUX. In this architecture, there is the use of an additional inverter in the XOR module to convert the XOR output to XNOR [8]-[11].

In the XOR module architecture which is utilized in this paper, the logic simplification is seen after we count the number of stages the output takes to be propagated. the fundamental design which when used took 3 stages to generate Cout, 4 stages to generate sum, and 5 stages to generate Carry. When this architecture is utilized then the number of stages of Cout was reduced from 3 to 2 for Sum from 4 to 3 and for Carry from 5 to 3. This shows that the reduced logical design for the compressor is effective in reducing the delay of the module.

3.Design

The architecture that inspired the design is the XOR-MUX architecture where there are three 2-input XOR modules and two 2x1 multiplexers [11]. The 2x1 multiplexer is designed using transmission gates as shown in Figure 6.

The XOR module is designed using 4 transistors. This module is then used along with the multiplexer module to implement a 4:2 compressor. The whole circuit uses a total of 28 transistors and is shown in Figure 5.

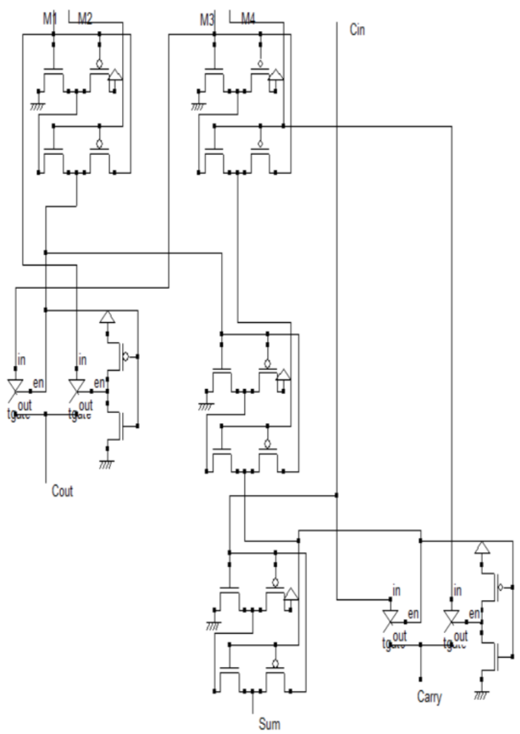

Fig 5: Proposed design of 4:2 Compressor

4.Implementation on Multipliers

The proposed design was then implemented on 4 to 8-bit multipliers. in all the designs the individual partial products were obtained using AND gates. These partial products are then supplied as an input to the array of compressors. In previous designs, the utilization of Full adders was done [1] rather than compressors. the utilization of compressors lowered the quantity of transistors which further translates to

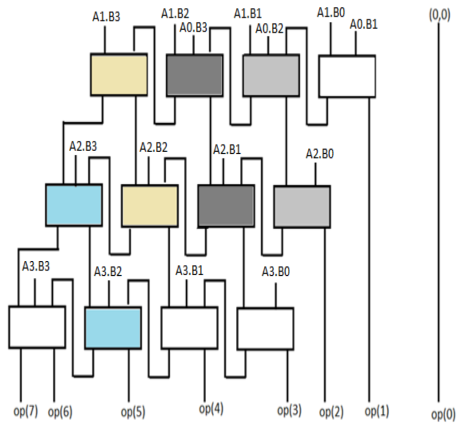

Fig 6: Design of a 4-bit array multiplier

lower power consumption by the device.

For example, if we take the 4-bit multiplier in Figure 6, initially the design that used 12 adder circuits has been reduced to a design that uses 4 adder circuits and 4 compressor circuits.

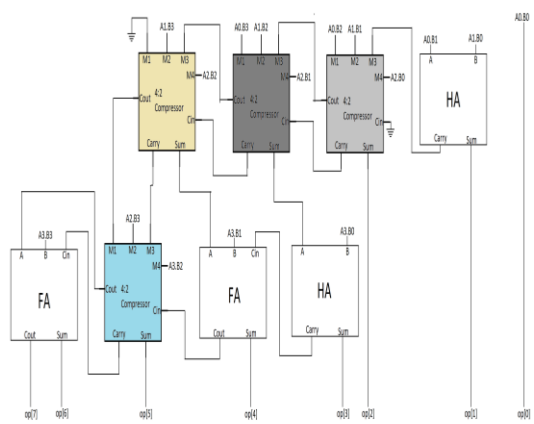

Fig 7: Design of 4 bit multiplier using 4:2 compressors

5.Result

The proposed compressor design has been verified using the Microwind tool where inputs were applied to M1, M2, M3, M4 & Cin and the corresponding outputs at Cout, Sum, and Carry were obtained. The outputs obtained were in accordance to the truth table. The input-output waveforms for the proposed design are in Figure 8.

The design showed a delay of 750ps for Carry, 450ps for Sum and 550ps for Cout. Thus, the maximum output delay of the module is 650ps. These results were obtained for 45nm design rules. The power

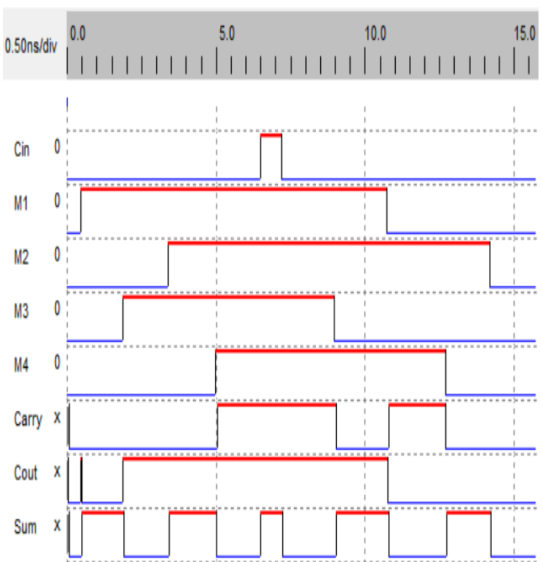

Fig 8: Input-Output waveforms obtained in proposed design

consumption of the module was too observed to be 10µW which is lower than the previous designs. The other designs for similar architecture showed a delay of at least 920.1ps [2]-[7]. The delay for the base design used in Figure 3 was 1310ps [1].

This design when implemented on a 4-bit multiplier was tested for maximum output delay it showed that the delay was 0.185ns whereas the design using adder circuits as shown in Figure 3 had a delay of 0.270ns. This shows that the design which used the proposed design of compressor used 0.085ns less i.e., 31% less than the basic design of array multiplier.

The number of transistors used by multipliers also drops by the use of the proposed design. The design of 4-bit multiplier using adders takes 408 transistors. The next best design in reference [2] when implemented on 4-bit multiplier takes 304 transistors. When the proposed design was used in implementation of 4-bit multiplier it took 264 transistors which is 35.3% less than the previous design and urea 13.2% less than reference [2]. The data related to the number of

Table 1: Propagation delay of proposed design

Output	**Delay** (in ns)
Cout	0.055
Carry	0.075
Sum	0.045

Table 2: Number of Transistors in 4-bit Multiplier using each design

	Module	**Transistors in each module**	**Total transistors**
Design in reference [1]	And	64	408
	Full Adder	288	
	Half Adder	56	
Design proposed in reference [2]	AND	64	304
	Full Adder	72	
	Compressor	144	
	Half Adder	24	
Proposed Design	And	64	264
	Full Adder	72	
	Compressor	112	
	Half adder	16	

modules and the transistors used in them has been provided in Table 2.

Similarly, the design was further implemented in the 5,6,7 and 8-bit multiplier. As shown in Table 3 the design leads to lowering the number of transistors used in the circuit.
Further analysis of the data showed that the drop in the number of transistors is more in odd bit multipliers the compressors designed are used to replace 2 successive adders. So, in odd bit multipliers as the number of successive adders is in even number the number of transistors reduced is higher. But as in an even bit multiplier, the successive adders are in odd numbers thus we have to add another layer of adders which lowers the drop in the transistor’s numbers.

6.Conclusion

In this paper, a new design for the 4:2 compressor is proposed which uses fewer transistors than its predecessors. With the reduction in transistors, the maximum output delay of the design has also reduced to 750ps for 45nm CMOS design. It also leads to a drop in the number of transistors in the compressor by 61%. This compressor when implemented on a multiplier will help in the reduction of the propagation delay and power consumption of the device.

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Table 3: Number of transistors utilised in each design

Bits	Array Multiplier	Proposed Design
4-bit	468	356
5-bit	790	478
6-bit	1196	796
7-bit	1686	954
8-bit	2260	1396

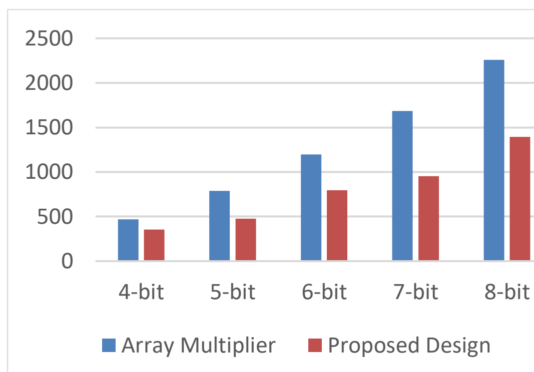

Fig 11: Comparison chart of transistors utilized in each multiplier

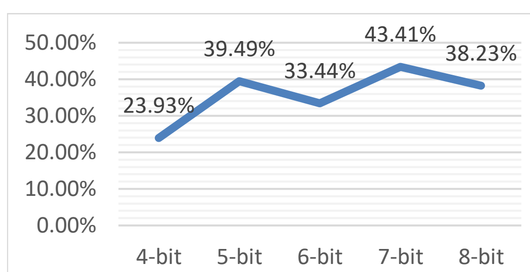

Fig 12: Chart depicting percentage drop in transistors utilized.

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