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Synthesis of CNFET based Multiplexer using Ternary Logic Circuits

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Abstract
Multi-Valued Logic (MVL) circuits have attracted the attention in recent times because of the advantages they offer in reducing the interconnect complexity and increasing the information content per unit area. Ternary Logic is a special case of MVL that has three logic levels. Implementation of voltage mode ternary logic circuits requires transistors with different threshold voltages. Carbon-Nanotube (CNT) is used as a conduction channel in CNFET and variations of the diameter of CNT results in variation in threshold voltage of CNFET. This property of CNFET makes it suitable for implementation of MVL circuits in general and ternary logic circuits in particular. In this paper, implement 2:1 multiplexer and decoder using ternary logic circuit. This technique is used to synthesize a set of benchmark ternary functions and the resulting circuits are compared with circuits synthesized using existing techniques.

Keywords
MVL, CNFET, Nano Device, Ternary Logic Gate

1. Introduction

Integrated circuit (IC) technology has enabled rapid advances in design and implementation of innovative devices, and systems that have changed the way we live and communicate. Integration of more transistors increases the computing power and helps in building efficient systems [1]. The number of transistors that can be integrated on a chip has been doubling every 1-2 years as predicted by the Gordon Moore, an industry pioneer, in 1960s [2]. This prediction, famously known as Moore's Law, has been proven correct, time and again. This has been made possible mainly due the continuous scaling or miniaturization of components that are integrated onto a chip [3]. For example, in CMOS technology, the gate length of a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) has been scaling by a factor of 0:7 every two years. Over the last few years, FinFET [4] (a variation of MOSFET) based devices have been fabricated at 22nm and the 14nm technology is foreseen to be reached in near future [5]. CMOS technology scaling beyond deep sub-micron/nano range, while enabling higher integration of VLSI designs, has caused various reliability issues. Some of the issues of CMOS scaling beyond nanometer range are increased leakage current, processes variations etc [6]. These non-idealities have caused the I-V characteristics of MOSFETs to be different from what is expected. It has become more difficult to improve performance by technology scaling.

CNFETs have been used widely in the implementation of ternary logic circuits. CNFET is one of the promising alternatives to MOSFET because of their exceptional one-dimensional band-structure that stifles backscattering and makes close ballistic activity a reasonable chance [7]. CNFETs utilize single walled CNT as a leading channel, which is directing or semiconducting relying upon the point of particle game plan along the cylinder additionally called as chirality vector. Unlike in MOS technology, where body biasing is used to control threshold voltages, in CNFET technology the threshold voltage is controlled by changing the diameter of CNT which in turn depends on the chirality vector. This dependence makes CNTFET suitable for implementation of MVL circuits.
There have been many CNFET-based design and synthesis techniques [8] that are used to realize ternary logic circuits. The existing work on CNFET-based ternary logic circuits is relatively recent and there is scope to explore new design techniques to realize efficient ternary circuits. Therefore in this thesis, new design and synthesis techniques, which aid in realizing efficient CNFET-based ternary logic circuits, have been investigated.

2. Ternary Logic

Binary logic, when given a significant third value is called ternary logic or three valued logic and functions realized with three values are called ternary logic functions. The values 0, 1 and 2 form the nomenclature to denote the ternary values in this work.
A function f(X) is defined as a ternary logic function mapping $\{0, 1, 2\}^n$ to $\{2, 1, 0\}^n$ where X is given by X_1, ……X_n. When X_i, X_j ϵ {0, 1, 2}, the basic operations of ternary logic can be defined as:

$$X_i + X_j = max\{X_i, X_j\} \quad (1)$$

$$X_i \cdot X_j = min\{X_i, X_j\} \quad (2)$$

Where equations (1) and (2) indicate OR and AND operations respectively for ternary logic [9]. Another important logic function in ternary logic is a ternary inverter. Table 2.1 shows the yields of various ternary inverters that are utilized in ternary rationale. Relating to every one of the yields three inverters are characterized in particular, Negative Ternary Inverter (NTI), Standard Ternary Inverter (STI) and Positive Ternary Inverter (PTI) separately. The rationale esteems expected for various voltage levels are appeared in Table 1 where, voltages 0, V dd=2 and V dd compare to rationale esteems 0, 1 and 2 individually.

Table 1: Ternary Inverters

Input x	NTI (x)	STI (x)	PTI (x)
0	2	2	2
1	0	1	2
2	0	0	0

Table 2: Logic Symbols

Voltage Level	Logic Value
0	0
$Vdd/2$	1
Vdd	2

Usage of ternary rationale circuits requires semiconductors with various edge voltages. Thus CNFET innovation, where the limit voltage of semiconductor can be altered by changing its physical measurements, is appropriate to execute ternary rationale circuits [8]. The accompanying area presents a concise outline of CNFET.

3. CNFET

A single-walled carbon nanotube (SWCNT) is obtained by rolling up a sheet of graphite along a roll-up vector C = na+mb, as shown in Figure 1, where m and n are positive integers which specify the chirality of the tube and 0a0 and 0b0 are lattice unit vectors [10].

The angle of atom arrangement along the tube, also called as chiral angle or roll-up vector or chirality vector in a single wall CNT (SWCNT), is represented by an integer pair (n;m). The value of (n; m) determines if CNT is metallic or semiconducting.

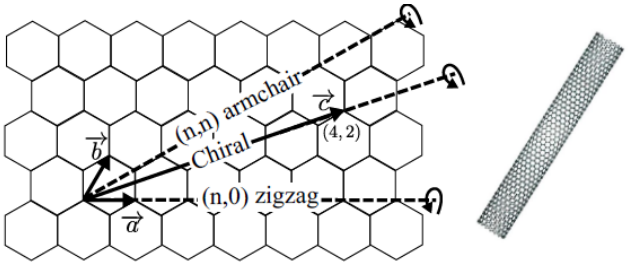

Figure 1: Unrolled sheet of graphite and the rolled lattice structure of CNT

SWCNT is further classified into three groups, depending on the angle of atom arrangement, i.e. chirality vector, along which the CNT is rolled. The three groups of CNT are named as armchair CNT if CNT has n = m, zigzag CNT if n = 0 or m = 0 and chiral CNT if m and n are different and nonzero. All armchair CNTs behave as conductors. On the other hand, zigzag and chiral CNTs show metallic (conducting) behavior when n = m or n–m = 3i, where i is an integer, otherwise they show semiconducting behavior. Hence zigzag and chiral CNTs are used in realizing a CNTFET. The chirality vector (n;m) also sets the diameter of the CNT. Carbon-Nanotube Field Effect Transistor (CNFET) is a transistor which makes use of semiconducting carbon nanotubes as channel material between two metal electrodes that act as source and drain contacts. The operating principle of CNFET is similar to that of MOS transistors. As shown in Figure 2, this three (or four) terminal device consists of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The drain current is directly proportional to the number of CNTs connected between the source and the drain and their respective diameters.

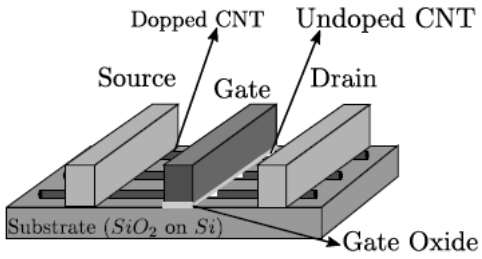

Figure 2: 3D view of Carbon-Nanotube Field Effect Transistor (CNFET)

Three types of CNTFET devices have been reported in the literature. They are known as schottky barrier CNTFET (SB-CNTFET), MOSFET-like CNTFET (M CNTFET) and band-to-band tunneling CNTFET (T-CNTFET). Due to the similarities of M-CNTFET with MOSFET in terms of operation and intrinsic attributes, it has been used in implementation of logic circuits.

4. Proposed Methodology and Result

Transistor Level Implementation

Another approach that uses unary operators and 3: 1 multiplexers for implementing ternary logic circuits has been presented.

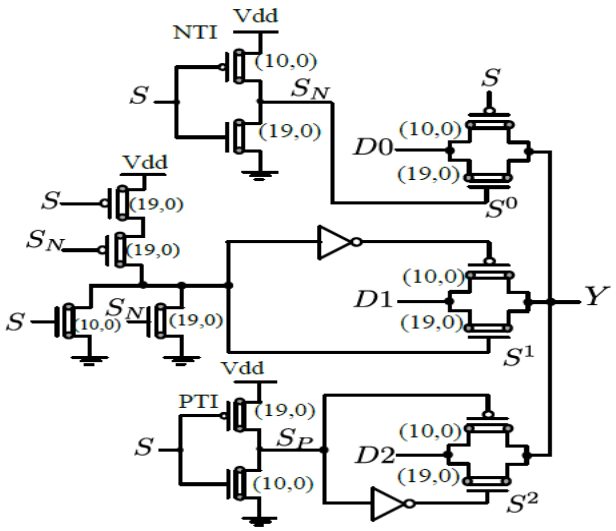

Figure 3: Transistor level Implementation of 3:1 Multiplexer

Since it has two inputs, one of the inputs is chosen as select line for a 3:1 multiplexer and the other input is used in generation of unary operators. If input A is chosen as the select signal and A = 0, then (0; 1; 2) is transformed into (0; 1; 1) with respect to input B.

Similarly when A = 1 or A = 2, (0; 1; 2) is transformed into (2; 0; 0) with respect to input B. These transformations, also called unary operators, have been implemented in such a way that they have low power consumption. Figure 3 illustrates the implementation using the 3:1 multiplexers and unary operators. This design requires 18 CNFETs as shown in Figure 3.

Binary Decision Diagram (BDD)

A binary decision diagram (BDD) is used to represent a two-valued logic function F. Let F = x*F_0 +x*F_1 be the Shannon expansion of F with respect to variable x. The BDD for F is represented as shown in Figure 4(a), where F_0 and F_1 represent the sub-graphs.

A BDD for a function F, whose truth table is known, is constructed by a procedure as shown in Figure 4(b) which has one-to-one correspondence between 2n rows of the table and the 2n paths to the outputs of the diagram. These outputs may then be labeled with the corresponding binary values of f resulting in the required diagram. Figure 4(c) also shows the implementation of BDD using 2:1 multiplexers. With n variables, there will initially be 2^n-1 nodes in a BDD. There are several ways in which the number of nodes can be reduced.

A	B	F
0	0	a
0	1	b
1	0	c
1	1	d

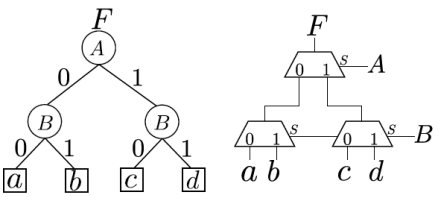

Figure 4: BDD and its 2:1 Mux based implementation for a given Truth-table

Ternary Decision Diagram (TDD)

A general-TDD is a natural extension of the BDD to the three-valued case. Let F = x_0*F_0 + x_1*F_1 + x_2*F_2 be the three-valued version of the Shannon expansion of an arbitrary three-valued function F : $T^n \rightarrow T$; T = {0; 1; 2} with respect to variable x.

The TDD for F is represented as shown in Figure 5(a), where F0, F1 and F2 represent the sub-graphs and the relation between values x0; x1; x2 and x is given by equation (3). As seen from this equation, the values x_0; x_1; x_2 are binary in nature and are equal to 2 or 0.

Similar to a BDD, the truth table for a function F can be translated into a TDD, which can be implemented using 3 : 1 multiplexers. Figure 5(b) shows an example truth table along with TDD and its implementation using multiplexers. With n variables, there will initially be 3^n-1/2 nodes in a TDD, which can be reduced. The decision diagrams with reduced nodes are called as Quasi Reduced TDD (QRTDD) or Reduced TDD (RTDD). Recently, a 3:1 multiplexer based synthesis procedure has been presented in. This procedure is similar to TDD based implementation (in Figure 5(c) except for the last stage, where the multiplexers were replaced with equivalent realization of unary operators.

A	B	F
0	0	a
0	1	b
0	2	c
1	0	d
1	1	e
1	2	f
2	0	g
2	1	h
2	2	i

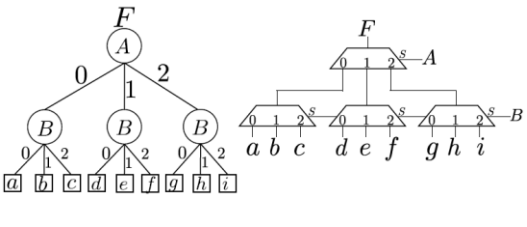

Figure 5: TDD and its 3 : 1 Mux based implementation for a given Truth-table

TBDD

The proposed synthesis technique for ternary logic circuits is based on transforming a TDD into a BDD. First, a general procedure to transform TDD to BDD is presented.

This enables the implementation of ternary logic circuits using 2:1 multiplexers. The transformed TDD is called as Ternary-Transformed Binary Decision Diagram (TBDD).

This TBDD representation is then used in the synthesis of ternary functions. Initially, TBDD-based synthesis techniques for handling one and two variable (2-input) functions are presented. These techniques are further used in synthesis of circuits with more than two inputs.

The graphs shown in Figure 6 can be implemented using 2:1 multiplexers. This implementation differs from multiplexer based implementation of

BDD, with respect to the selection signal. Here, the selection signal is three-valued and hence there should be a way to differentiate between three possible values i.e. 0, 1 and 2. This can be achieved for TBDD representation by passing the selection signal through the NTI and PTI gates. But for implementation of TBDD a NOR like structure is needed to generate x_1 and $x_{1'}$ which increases the complexity. Hence, in this work, only TBDDs represented in Figures 6(a) and 6(b) is used.

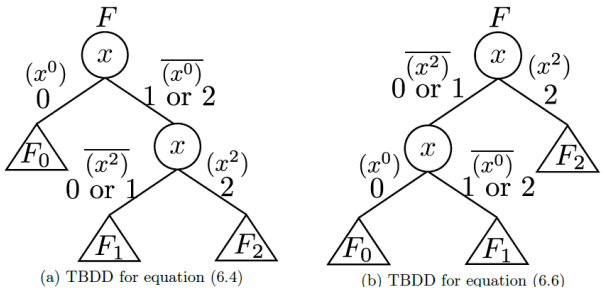

Figure 6: Ternary-Transformed Binary Decision Diagram

To differentiate between the two different multiplexers, 2:1 multiplexer with NTI gate is referred as NTI-Mux and the one with PTI gate is referred as PTI Mux.

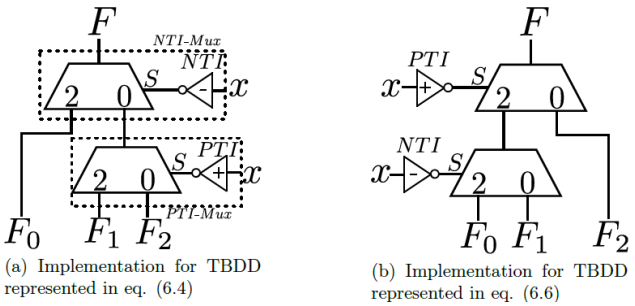

Figure 7: 2:1 Multiplexer based implementation of TBDD

5. Conclusion

In this work we presented a novel synthesis technique to implement ternary logic circuits using "2:1 multiplexers". This technique uses a transformation which converts a ternary decision diagram (TDD) in to binary decision diagram (BDD). This transformed TDD is then used to implement the ternary logic function using 2:1 multiplexers.
A procedure to decompose ternary functions with three (or more) inputs to multiple 1-input ternary functions has also been presented in this work. This procedure is developed into a synthesis algorithm, which is further used in the synthesis of benchmark ternary functions. Synthesis results of these functions indicate that the proposed algorithm results in circuits that have, on an average, 79% and up to 99% less transistors when compared to the existing 3:1 multiplexer based designs.

REFERENCES

[1] Muhammad Ali, Mohammed Abrar Ahmed, and Malgorzata Chrzanowska-Jeske, "Logical Effort Framework for CNFET-Based VLSI Circuits for Delay and Area Optimization", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018.

[2] S. I. Sayed, M. M. Abutaleb, and Z. B. Nossair, "Optimization of CNFET parameters for high performance digital circuits," Adv. Mater. Sci. Eng., vol. 2016, Jul. 2016, Art. no. 6303725.

[3] M. Ali, M. Ahmed, and M. Chrzanowska-Jeske, "Fast and accurate evaluation of delay in CNFET circuits," in Proc. IEEE 16th Int. Conf. Nanotechnol. (IEEE-NANO), Aug. 2016, pp. 659–662.

[4] M. Ali, M. Ahmed, and M. Chrzanowska-Jeske, "Stochastic analysis of CNFET circuits using enhanced logical effort model in the presence of metallic tubes," in Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS), Dec. 2014, pp. 774–777.

[5] M. Ali, R. Ashraf, and M. Chrzanowska-Jeske, "Logical effort of CNFET-based circuits in the presence of metallic tubes," in Proc. 12th IEEE Int. Conf. Nanotechnol. (IEEE-NANO), Aug. 2012, pp. 1–6.

[6] G. Cho, Y. B. Kim, and F. Lombardi, "Modeling Undeposited CNTs for CNTFET Operation," IEEE Trans. Device Mater. Rel., vol. 11, no. 2,bbpp. 263–272, Jun. 2011.

[7] B. Ghavami and M. Raji, "Failure characterization of carbon nanotube FETs under process variations: Technology scaling issues," IEEE Trans. Device Mater. Rel., vol. 16, no. 2, pp. 164–171, Jun. 2016.

[8] R. Ashraf, M. Chrzanowska-Jeske, and S. G. Narendra, "Functional yield estimation of carbon nanotube-based logic gates in the presence of defects," IEEE Trans. Nanotechnol., vol. 9, no. 6, pp. 687–700, Nov. 2010.

[9] S. Karmakar, J. A. Chandy, and F. C. Jain, "Design of ternary logic combinational circuits based on quantum dot gate fets," IEEE Trans. Very Large Scale Integr. Syst., vol. 21, no. 5, pp. 793–806, May 2013.

[10] D. Mateo and A. Rubio, "Design and implementation of a 5 times;5 trits multiplier in a quasi-adiabatic ternary cmos logic," IEEE Journal of Solid-State Circuits, vol. 33, no. 7, pp. 1111–1116, Jul 1998.

[11] S. Lin, Y. B. Kim, and F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits," IEEE Transactions on Nanotechnology, vol. 10, no. 2, pp. 217–225, March 2011.