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LOW POWER AND LOW PDP TERNARY ADDER DESIGN BASED ON CNTFET TECHNOLOGY

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Abstract

Electronic devices portability requires major low power requirements and also high-speed requirements so there is high necessity for improving the circuits. Ternary logic these days is in high demand as most special algorithms such as fuzzy logic works on ternary logic so there is necessity of improving the performance of the ternary adder. In this thesis, we have proposed a new approach for Ternary Adder, in which tri-mode technique is used to improve the performance of the circuit and compared with a sleep transistor-based technique and the simple ternary adder. With this improvement it is seen that the proposed circuits give better performance in terms of Average Power, Delay, PDP and EDP. So, tri-mode technique and sleep mode technique have higher advantages in terms of performance metrics calculated. CNTFET has a high performance in terms of performances and is a better substitute for MOSFET in 32nm technology.

***Keywords*- Electronic device, Circuits, transistor, PDP and EDP, CNTFET.**

1.NTRODUCTION

As indicated by Moore's law the elements of individual devices in a coordinated circuit have been diminished by a factor of around two at regular intervals. This downsizing of devices has been the main impetus in innovative advances since the late twentieth century. In any case, as substantiated by ITRS 2009 release, further downsizing has confronted genuine limits identified with manufacture innovation and device exhibitions as the basic measurement contracted down to sub-22 nm range. The points of confinement include electron burrowing through short channels and slight protector films, the related leakage currents, aloof power dissipation, short channel effects, and varieties in device structure and doping. These breaking points can be defeated to some degree and encourage further downsizing of device measurements by altering the channel material in the conventional mass MOSFET structure with a solitary carbon nanotube or a variety of carbon nanotubes. Electronic device, innovation and circuit specialists are investigating conceivable options for the fate of semiconductor industry to improve execution of electronic framework. Research is being completed in growing high-portability transistor channel materials, for example, compound semiconductors, stressing the channel material to improve bearer versatility just as in utilizing non planar transistor structures in particular CNTFETs and multi gate structures. All the while, novel one-dimensional structures e.g., nano wires and carbon nano tubes (CNTs) are additionally being effectively inquired about. CNTs, with their predominant transporter portability, have developed as a potential possibility to help the Si innovation guide in a post 2015-time allotment, albeit various difficulties remain [1]. Subsequently, carbon nano tube field-effect transistors (CNTFETs) give chance to look into at both device and circuit levels. Silicon based innovation will achieve its

cut off points in 2020 when the channel length of MOSFET is beneath 10nm. Hence, the semiconductor business is searching for various materials and devices to incorporate with the current silicon-based innovation or possibly, in a long-haul future, even substitute it. Among the quantity of investigated arrangements, for example, single-electron burrowing (SET), fast single-transition quantum rationale, quantum cell automata (QCA) and carbon nano tubes (CNT), CNTs are a promising material. They have widths of ordinarily 1 to 3 nm, yet being long up to a few microns. CNTs can be misused to manufacture both low — opposition high-quality interconnections and very adaptable low-power carbon nano tube field-effect transistors (CNTFET) and single electron burrowing transistors [1]. By and by, many research groups carry out investigations about CNTFET devices and their rationale applications everywhere throughout the world, both in mechanical labs (IBM, Intel, Infineon,) and in colleges (Purdue, Stanford,). One of the essential thoughts is to supplant the silicon MOSFETs with CNTFETs to defeat every one of the restrictions of silicon MOSFETs. Be that as it may, the plan of circuits dependent on such devices requires accessible device models, perfect with exceptional structure streams. This work gives an outline of current kinds of CNTFETs and of some minimized models. Utilizing the accessible models, the impact of the parameters on the device attributes was recreated and broke down. The end is that the cylinder breadth impacts the current dimension, yet additionally the edge voltage of the CNTFET, while the contact opposition impacts just the current dimension. From a planner's perspective, dealing with the parameter varieties and specifically of the nano tube distances across is essential to accomplish solid circuits.

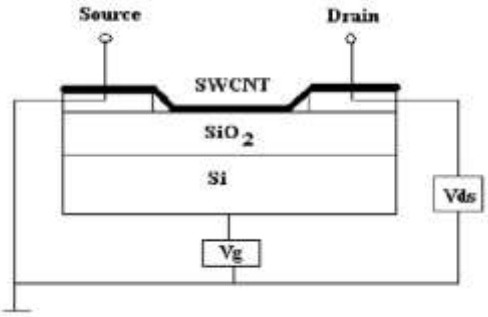

Figure 1: Back Gate CNTFET

Carbon Nanotube Field Effect Transistors (CNTFET) are promising Nano-scaled devices for executing elite thick and low power circuits. A Carbon Nanotube Field Effect Transistor alludes to a FET that uses a solitary CNT or a variety of CNT's as the channel material rather than mass silicon in the conventional MOSFET structure. The centre of a CNTFET is a carbon nanotube. In this work, the audit of CNTFETs is introduced. The structure, activity and the qualities of various kinds of CNTFET's have been talked about. The task, dc attributes of CNTFETs have been introduced and examination of the execution of different qualities These were straightforward devices manufactured by saving single-divider CNTs (orchestrated by laser removal) from arrangement onto oxidized Si wafers which had been prepattemed with gold or platinum terminals. The anodes filled in as source and drain, associated by means of the nanotube channel, and the doped Si substrate filled in as the gate. A schematic of such a device is appeared in Figure.1.2. Clear p-type transistor activity was watched, with gate voltage regulation of the drain current more than a few requests of extent. The devices showed high on-state obstruction of a few MQ, low Trans conductance (- Ins) and no current immersion, and they required high gate voltages (a few volts) to turn them on.

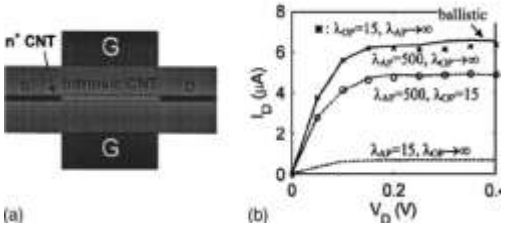

Figure 1.2: Early CNTFET Structure

2.LITERATURE SURVEY

Kazi Muhammad Jameel et al [2], "Exploratory Design of a Ternary Full Adder utilizing Pseudo N-type Carbon Nano tube FETs" A full adder is a vital segment of a number juggling circuit. Expanding the dimension of rationale in an Adder circuit results in more productivity as it can register bigger numbers with more prominent precision. In this paper a ternary adder is structured with ternary rationale. The

usage of the structure depends on Pseudo n-Type carbon nano tube field effect transistors. This paper demonstrates the investigation of the ternary full adder and assesses the plan contingent upon its power consumption, deferral and power postpone item.

Shimaa I. Sayed et al [3], "A Novel High-speed Adder-Sub tractor Design dependent on CNFET" Carbon Nanotube documented effect transistor (CNFET) is one of the promising options in contrast to the MOS transistors. The geometry subordinate edge voltage is one of the CNFET attributes, which is utilized in the proposed plan. In this paper, we present a novel fast Adder-sub tractor cell utilizing CNFETs dependent on XOR gates and multiplexer. Exhibited configuration utilizes fourteen transistors, ten for full adder and four to alter the cell for subtraction. Re-enactment results show critical improvement as far as deferral and region sparing with 48% and 11% individually contrasted with the most recent structure. Recreations were done utilizing HSPICE dependent on CNFET show with streamlined plan parameters.

Andreas Heregeld and Siegbert Hentschke et al [4], "Ternary Multiplication Circuits Using 4-Input Adder Cells and Carry Look-Ahead" We present another usage of a ternary adder with four inputs and two outputs. This ternary adder diminishes the quantity of digits in an increase contrasted and a double duplication. One preferred standpoint of the ternary adder is that four rather than three inputs inside a parallel portrayal will be summed up. In this paper we will look at the multifaceted nature of paired against ternary multipliers. Timing graphs will be given for the twofold and the ternary case with an ideal request of the adder inputs. At last, we present a ternary carry look-ahead circuit for a further decrease of all out-time delay.

3.METHODOLOGY

The current two plans and the past announced structure are actualized by HSPICE utilizing CNTFET show. In this model, the Schottky effect is dealt with, by picking suitable qualities for the parameters Sout and Dout speaking to source/drain availability. Every one of the three structures are recreated broadly at room temperature with 0.9 V supply voltage and 1 GHz recurrence. The transient reaction of the circuit is appeared in the Figure 3.13. All input signs have an ascent time and a fall time of 20ps. A run of the mill rise time delay tr1 is appeared in Figure 3.13. This is estimated when input An is ascending from 0 to 1 and the Sum is changing from 0 to 1. Comparable method is pursued to acquire all conceivable ascent time deferrals and fall time delays for Sum and Carry. The average of every one of those postponements is considered as the deferral of the circuit and noted in Table3.6. The average powers consumed by the circuits are likewise revealed in Table 3.6. At that point utilizing these two execution parameters the power defer item is gotten for each plan and recorded in Table 3.6. The examination of the table demonstrates that for the current plans, the circuit multifaceted nature is not exactly the past announced structure. The transistor tally of Design1 is decreased from 130 to 94. This plan additionally consumes 12% less power with less deferral. The PDP is diminished by 15%. The Design2 with new decoder utilizes just 66 transistors. The decreases in deferral, power and PDP for this structure are 9%, 63% and 66% separately, contrasted with the prior detailed plan.

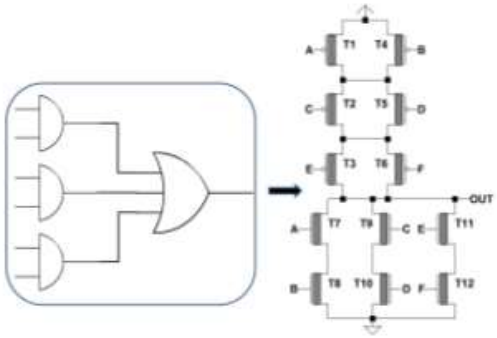

Figure 3.13: Transistor level implementation of 3 AND 1 OR gate.

Circuit Type	Transistor Count	Delay (psec)	Percentage improvement of delay w.r.t. [5] (%)	Power (nW)	Percentage improvement of power w.r.t. [5] (%)	PDP $\times 10E^{-17}$J	Percentage improvement of PDP w.r.t. [5] (%)
Lin [5]	130	18.09		673.06		1.2176	
*Design*1	94	17.62	2	588.63	12	1.0372	14.8
*Design*2	66	16.52	9	249.06	63	0.4114	66

Table 3.6: Performance Comparison

4. IMPLEMENTATION AND RESULTS

Waveform of CNTFET based Ternary Adder

Ternary Adder waveform is given for CNTFET based Ternary Adder in 32nm technology.

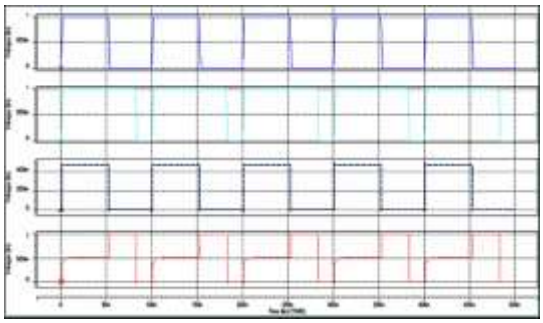

Figure 4.1: Waveform of CNTFET based Ternary Adder

Proposed Tri mode Ternary Half Adder using CNTFET

In figure 4.2, the circuit for ternary half adder using tri mode technique is presented. In this circuit, in the ground network, two transistors are added as seen in the figure. And the gate of two transistors is connected to sleep and hold signals. Hence, its requirement is to save power with keeping it up to output expectations even when the circuit is in sleep mode. Other signal here is hold. Sleep and hold controls when the circuit is in sleep mode or hold mode.

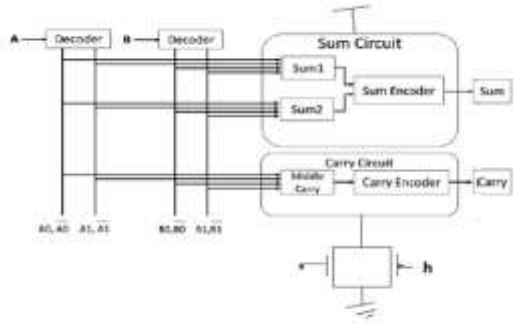

Figure 4.2: Proposed TMTHA using CNTFET

Proposed Sleep Transistor Ternary Half Adder using CNTFET

This technique is shown in Figure 4.3. it has two transistors when connected to Vdd and other NCNTFET to ground. The signal sleep and sleep bar control the outputs of the circuit.

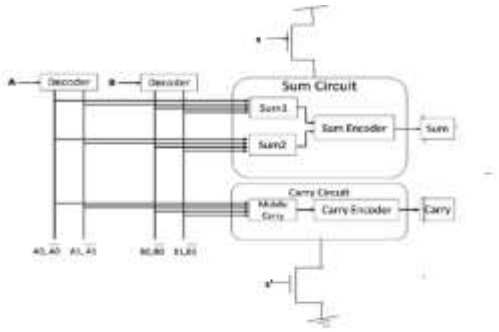

Figure 4.3: Sleepy Ternary Adder Technique

Simulation Results for Proposed Circuits with Ternary Adder

	Ternary Adder	Tri Mode	Sleep Mode
Average Power	3.27E-05	1.09E-05	4.01E-06
Delay	3.00E-08	3.04E-08	3.02E-08
PDP	9.83E-13	3.33E-13	1.21E-13
EDP	2.95E-20	1.01E-20	3.66E-21

Table 4.1: Simulation output parameters

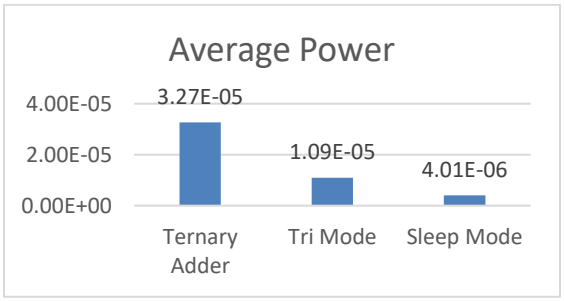

Figure 4.4: Average Power for Tri-mode, Sleep Mode and Base TA

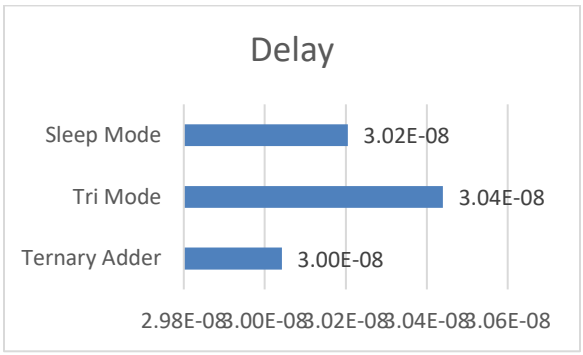

Figure 4.5: Delay for Tri-mode, Sleep Mode and Base TA

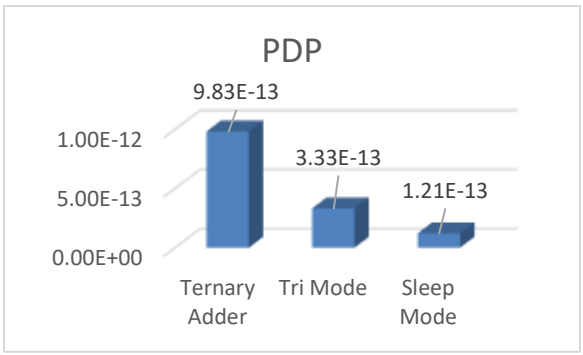

Figure 4.6: PDP for Tri-mode, Sleep Mode and Base TA

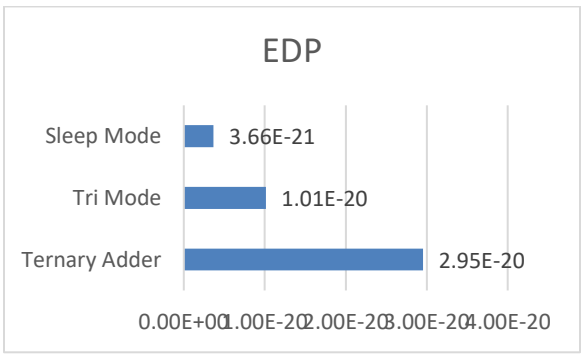

Figure 4.7: EDP for Tri-mode, Sleep Mode and Base TA

4. CONCLUSION

Hence, we conclude in this section, that tri-mode and sleep techniques work well with ternary adder circuit. The Average Power is improved by 66.6% in tri-mode and 88.7% in sleep mode, delay is nearly same in all circuits, PDP is improved by 66.1% in tri-mode and 87.6% in sleep mode. Also, energy is improved by 65.7% in tri-mode and 87.5% in sleep mode technique. Hence both the new techniques are performing good. Also, tri-mode is generally used for low noise applications.

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