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Design and implementation of BCD adder and subtractor using programmable reversible gates

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Abstract
Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. Arithmetic unit design using reversible logic gate has received much attention as it reduces power dissipation with no loss of information. This paper proposes the design of 32-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 32 -bit BCD addition unit is designed using the following modules such as reversible 4-bit Carry Propagate unit using reversible logic gates such as Feynman gate and URG gate and a reversible 4-bit error correction unit. The 4-bit error correcting unit designed by reversible (4x1) Multiplexer (MUX) unit using Toffoli gate and TNOR gates to provide the output with a precise value. The reversible 32-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. The proposed design is synthesized using Xilinx ISE software and simulated using VHDL test bench.

Keywords
Reversible gates, Adder/sub tractor, Garbage output, Quantum cost .

1.Introduction
In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n –input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. In this paper, we design a 16 bit reversible ALU that can perform eight operations simultaneously. The eight operations include addition, subtraction, AND, NAND, OR, NOR and XOR. All the modules are simulated in modalism SE 6.5 and synthesized using Xilinx ISE 14.1.

2.Literature survey
The research on reversible logic is being pursued towards both design and synthesis. In the synthesis of reversible logic circuits there has been several interesting attempts in the literature such as the work in [2-3]. A reversible arithmetic logic unit was designed by Thomsen, Gluck, and Axelsen [4] that was based on the V-shaped design of the Van Rentergem adder [5]. The ALU had five fixed select lines, and produced the following logical outputs: ADD, SUB, NSUB, XOR and NOP. The least significant bit comprised of two Feynman gates and two Toffoli gates. Each additional bit also had two Fredkin gates.

Ms. A. Anjana et al. [6], arithmetic unit design using reversible logic gate has received much attention as it reduces power dissipation with no loss of information. This paper proposes the design of 32-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 32 -bit BCD addition unit is designed using the following modules such as reversible 4-bit Carry Propagate unit using reversible logic gates such as Feynman gate and URG gate and a reversible 4-bit error correction unit. The 4-bit error correcting unit designed by reversible (4x1) Multiplexer (MUX) unit using Toffoli gate and TNOR gates to provide the

output with a precise value. The reversible 32-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. In BCD subtraction unit, the error correcting block is designed with the conditional reversible logic COG gate to make the necessary corrections at the output to get exact output. The reversible 32bit BCD addition and subtraction unit is designed based on the parallel pipelined unit to enhance the speed of operation. This proposed reversible 32-bit BCD addition module has 416 garbage values with the critical path delay of 17.420 ns; reversible 32-bit BCD subtraction module has 240 garbage values with the critical path delay of about 17.420 ns.

Asher Peres: This article is concerned with the construction of a quantum-mechanical Hamiltonian describing a computer. This Hamiltonian generates a dynamical evolution which mimics a sequence of elementary logical steps. This can be achieved if each logical step is locally reversible (global reversibility is insufficient). Computational errors due to noise can be corrected by means of redundancy. In particular, reversible error-correcting codes can be embedded in the Hamiltonian itself. An estimate is given for the minimum amount of entropy which must be dissipated at a given noise level and tolerated error rate[7].

Raghava Garipelly et al."A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering in this paper the Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs[8-11]. This paper provides the basic reversible logic gates, which in designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible. Thispaper presents the data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates.
Himanshu Thapliyal et al. "Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate", 2009 IEEE Computer Society Annual Symposium on VLSI, this paper tells about the extensive applications of Reversible logic in quantum computing, low power VLSI design, quantum dot cellular automata and optical computing. While several researchers have investigated the design of reversible logic elements, there is not much work reported on reversible binary subtractors. In this paper, we propose the design of a new reversible gate called TR gate. Further, we investigate the design of reversible binary subtractors based on the proposed TR gate. The proposed TR gate is better for designing reversible binary subtractor compared to such gates discussed in literature in terms of quantum cost, garbage outputs and complexity of gates.

Morrison, M. et al. "Design of a novel reversible ALU using an enhanced carry look- ahead adder" Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference Reversible logic is gaining significant consideration as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Recent advances in reversible logic allow schemes for computer architectures using improved quantum computer algorithms. Significant contributions have been made in the literature towards the design of reversible logic gate structures and arithmetic units, however, there are not many efforts directed towards the design of reversible ALUs. In this work, a novel programmable reversible logic gate is presented and verified, and its implementation inthe design of a reversible Arithmetic Logic Unit is demonstrated. Then, reversible implementations of ripple-carry, carry-select and Kogge-Stone carry look-ahead adders are analyzed and compared. Next, implementations of the Kogge-Stone adder with sparsity-4, 8 and 16 were designed, verified and compared. The enhanced sparsity-4 Kogge-Stone adder with ripple-carry adders was selected as the best design, and its implemented in the design of a 32-bit arithmetic logic unit is demonstrated.

3.Reversible gates

Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional

AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table shown in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed[12-15]. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

- **Basic reversible gates**

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available and is commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions.

- **Basic reversible gates**

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

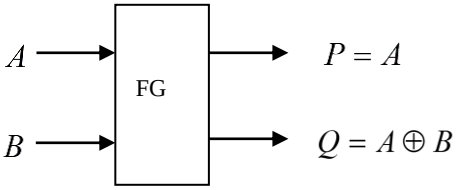

Figure 1 Feynman gate

In Figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

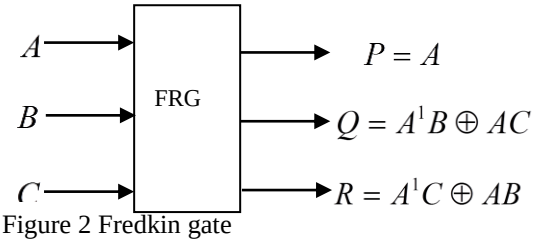

Figure 2 Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities not withstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

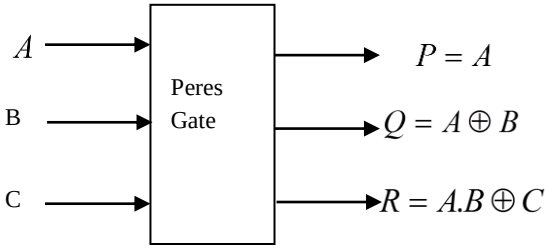

Figure 3 Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$
$$Q = B \quad (2)$$
$$R = A \oplus B \oplus C \quad (3)$$
$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Figure 4.

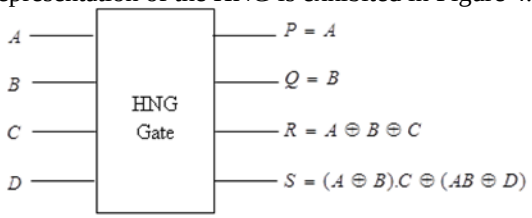

Figure 4 Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$
$$Q = A \oplus B \quad (6)$$
$$R = AB \oplus C \quad (7)$$
$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Figure 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

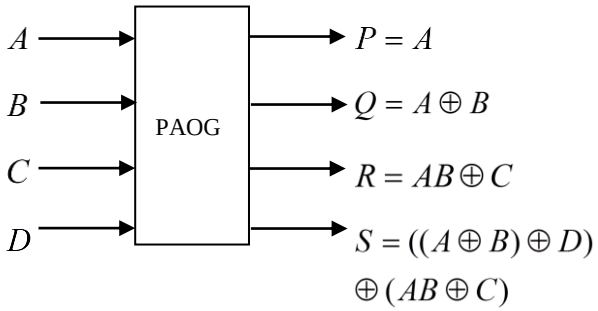

Figure 5 Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

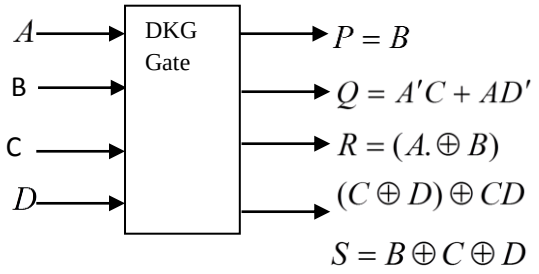

Figure 6 DKG Gate

$$P = B \quad (9)$$

$$Q = A'C + AD' \quad (10)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

4.Proposed methodology

BCD binary numbers represent Decimal digits 0 to 9. A 4-bit BCD code is used to represent the ten numbers 0 to 9. Since the 4-bit Code allows 16 possibilities, therefore the first 10 4-bit combinations are considered to be valid BCD combinations. The latter six combinations are invalid and do not occur BCD Code has applications in Decimal Number display System such as counters and digital clock. BCD numbers can be added together using BCD addition.

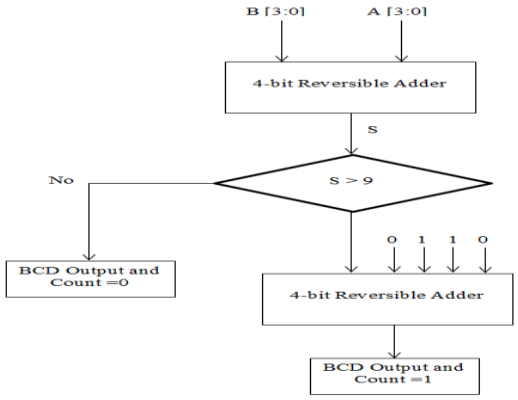

Figure 7 Proposed 4-bit reversible BCD Addition unit

Decimal BCD Subtractor – Addition of signed BCD numbers can be performed by using 9's or 10's complement methods. A negative BCD number can be expressed by taking the 9's or 10's complement. Let us see 9's and 10's complement numbers and subtraction process using it. The 9's complement of a decimal number is found by subtracting each digit in the number from 9. The 9's complement of each of the decimal digits.

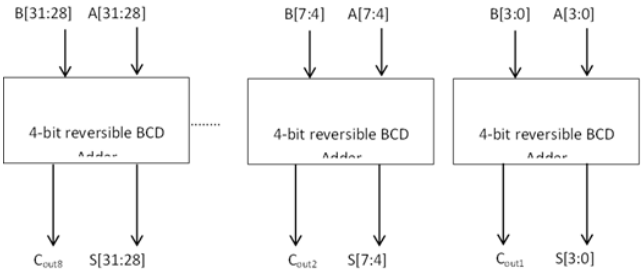

Figure 8 Flow Chart of 32-bit Reversivle BCD Adder

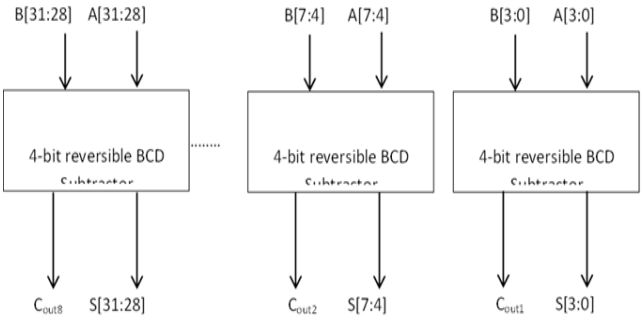

Figure 9 Flow Chart of 32-bit Reversible BCD Subtractor

By casding 8 reversible 4-bit adder using peres gate along with the carry out. 32-bit reversible BCD addition can be relized as shown in figure 39. By casding 8 reversible 4-bit subtractor using TR gate along with the carry out. 32-bit reversible BCD subtractor can be relized as shown in Figure 9.

Table 1 Device utilization of different BCD Design

4-bit			
Parameter	BCD Adder using peres Gate	BCD Sub-tractor using TR Gate	BCD Adder/Sub-tractor using DKG Gate
Number of Slice LUTs	9	12	9
Number of Bounded IOBs	13	16	14
MCPD(ns)	7.741	7.839	7.998
32-bit			
Number of Slice LUTs	72	128	72
Number of Bounded IOBs	104	104	105
MCPD(ns)	7.741	7.839	8.525
64-bit			
Number of Slice LUTs	144	256	144
Number of Bounded IOBs	208	208	209
MCPD(ns)	7.741	10.906	8.525

5.Conclusion

In this thesis, the design of 32-bit BCD add- subtract unit have been implemented using reversible logic gates. Modules such as 4-bit BCD addition, error correction unit, (4x1) MUX, conditional statements, 4-bit nine‟s complement unit have been designed using the reversible logic gates. BCD arithmetic units are speedy manipulation with reduced area. The four bit BCD addition is designed in the CPA fashion to further enhance the speed of 32-bit BCD arithmetic design for add- subtract units. 32-bit subtraction unit have been designed using 4-bit nine‟s complement and 4- bit BCD addition unit. The proposed module has wide range of application in digital signal processing. The estimated parameters for reversible 32-bit BCD addition unit is about 416 garbage values with the critical path delay of 17.420 ns; reversible 32-bit BCD subtraction module is about 240 garbage values with the critical path delay of about 17.420 ns.

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